



Attorney's Docket No.: 10559-075002/P7567C

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Matthew J. Adiletta Art Unit: 2183
Serial No.: 10/615,500 Examiner: R. Ellis
Filed : July 8, 2003
Assignee : Intel Corporation
Title : PARALLEL PROCESSOR ARCHITECTURE

Mail Stop Amendment

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Applicants call attention to the attached Information Disclosure Statement and documents listed on form PTO-1449.

Copies of the U.S. patents/publications are not being provided per the waiver posted on the PTO website.

Kindly accept this Information Disclosure Statement under Rule 97(c)(2). The rule 17(p) certification fee of \$180 is enclosed.

The documents are in the English language; hence no concise explanation is necessary per Rule 98(a)(3).

06/29/2005 HTECKLU1 00000001 10615500

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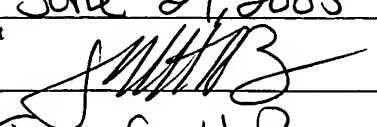
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Applicant : Matthew J. Adiletta
Serial No.: 10/615,500
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Page 2 of 2

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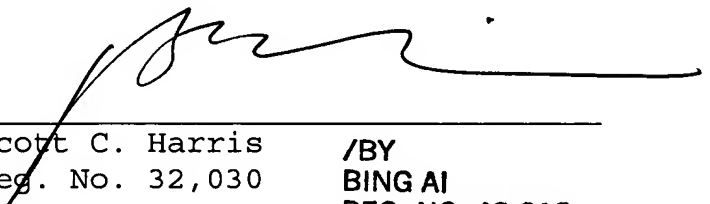
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Respectfully submitted,

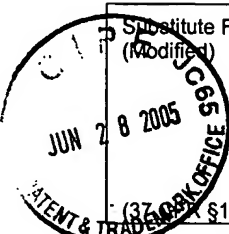


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 Attorney's Docket No.
 10559-075002

 Application No.
 10/615,500

**Information Disclosure Statement
 by Applicant**

(Use several sheets if necessary)

 Applicant
 Matthew J. Adiletta

 Filing Date
 July 8, 2003

 Group Art Unit
 2183

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	4,016,548	04/1977	Law, et al.			
	AB	4,032,899	06/1977	Jenny, et al.			
	AC	4,075,691	02/1978	Davis, et al.			
	AD	4,788,640	11/1988	Hansen			
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	AI	5,701,434	12/1997	Nakagawa			
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	AS	6,170,051	01/2001	Dowling			
	AT	6,212,542	04/2001	Kahle, et al.			
	AU	6,223,274	04/2001	Catthoor, et al.			
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	AZ	6,463,072	10/2002	Wolrich, et al.			
	AAA	6,463,480	10/2002	Kikuchi, et al.			

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Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-075002	Application No. 10/615,500
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Matthew J. Adiletta	
		Filing Date July 8, 2003	Group Art Unit 2183

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	ABB	6,463,527	10/2002	Vishkin			
	ACC	6,466,898	10/2002	Chan			
	ADD	6,529,983	03/2003	Marshall, et al.			
	ABE	6,535,878	03/2003	Guedalia, et al.			
	AFF	6,584,522	06/2003	Wolrich, et al.			
	AGG	6,587,906	07/2003	Wolrich, et al.			
	AHH	6,604,125	08/2003	Belkin			
	AII	6,606,704	08/2003	Adiletta, et al.			
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	AKK	6,661,794	12/2003	Wolrich, et al.			
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	AMM	6,671,827	12/2003	Guilford, et al.			
	ANN	6,792,488	09/2004	Wolrich, et al.			

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AOO							

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	APP	"10-/100-Mbps Ethernet Media Access Controller (MAC) Core", NEC, 1998, pages 1-5.
	AQQ	"Nomadic Threads: A migrating multithread approach to remote memory accesses in multiprocessors", by Jenks, S.; Gaudiot, J.L. (abstract only) Publication Date: 20-23 Oct. 1996.
	ARR	"Overview of the START (*T) multithreaded computer" by Beckerie, M.J. (abstract only) Publication Date: 22-26 Feb. 1993.
	ASS	A. Ippoliti, et al., "Parallel Media Access Controller for Packet Communications at Gb/s Rates", 1990, IEEE, pages 991-996.
	ATT	Howard Frazier, "Gigabit Ethernet: From 100 to 1,000 Mbps", 1999, IEEE Internet Computing, pages 24-31.
	AUU	Howard Frazier, "The 802.3z Gigabit Ethernet Standard", 1998, IEEE Network, pages 6-7.

Examiner Signature	Date Considered
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